1. Description

- SGT MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

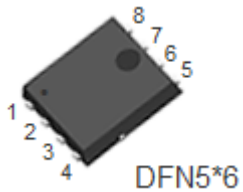
2. Features

- $R_{DS(ON)}$=2.4mΩ (typ.) @ V_{GS}=10V
- 100% UIS Tested
- 100% ▽V_{DS} Tested

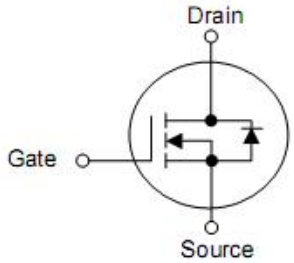
3. Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

4. Pin configuration



DFN5*6



Pin	Function
1,2,3	Source
4	Gate
5,6,7,8	Drain

5. Ordering Information

Part Number	Package	Brand
KCY3206B	DFN5*6	KIA

6. Absolute maximum ratings

TC=25℃ unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V_{DSS}	60	V
Gate-to-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon limited)		I_D	155	A
Continuous Drain Current [1]	T_C=25°C	I_D	95	A
	T_C=100°C	I_D	60	A
Pulsed Drain Current [2]		I_{DM}	390	A
Avalanche Energy [3]		EAS	500	mJ
Total Power Dissipation [4]		P_D	120	W
Operation Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

7. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.04	°C/W
Thermal Resistance, Junction-to-Ambient [5]	$R_{\theta JA}$	20	°C/W

8. Electrical characteristics

(T_J=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	1.6	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	2.4	2.8	mΩ
		V_{GS}=4.5V, I_D=15A	-	2.7	3.4	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V	-	-	1.2	V
Maximum Body-Diode Continuous Current	I_S		-	-	95	A
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=100KHZ	-	5960	-	pF
Output Capacitance	C_{oss}		-	1260	-	pF
Reverse Transfer Capacitance	C_{rss}		-	90	-	pF
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V, I_D=50A	-	95	-	nC
Gate-Source Charge	Q_{gs}		-	19	-	nC
Gate-Drain Charge	Q_{gd}		-	16	-	nC
Reverse Recovery Chrage	Q_{rr}	I_F=25A, di/dt=100A/us	-	75	-	nC
Reverse Recovery Time	t_{rr}		-	70	-	ns
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=30V, I_D=25A,R_{GEN}=2Ω	-	23.5	-	ns
Turn-on Rise Time	t_r		-	6.9	-	ns
Turn-off Delay Time	$t_{d(off)}$		-	80.5	-	ns
Turn-off fall Time	t_f		-	27.5	-	ns

Notes:
1). The maximum current rating is package limited.
2). Repetitive rating; pulse width limited by max. junction temperature.
3). V_{DD}=50 V, R_G=25Ω, L=0.5mH, starting T_j=25°C.
4). P_D is based on max. junction temperature, using junction-case thermal resistance.
5). The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25°C.

9. Typical Characteristics

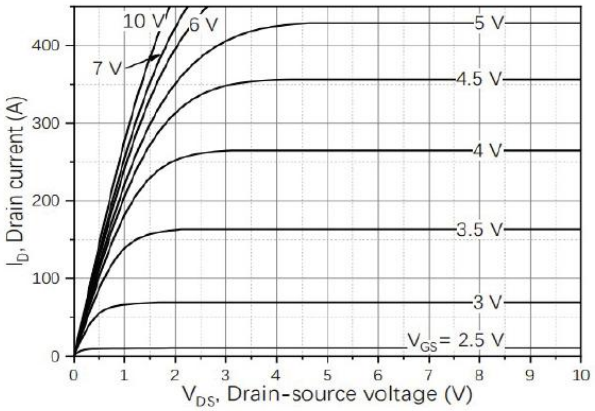


Figure1. Output Characteristics

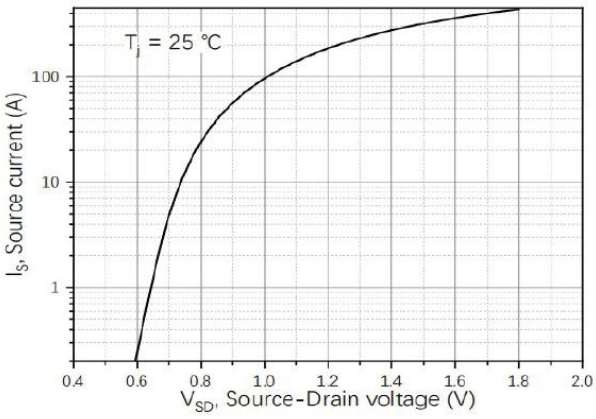


Figure2. Transfer Characteristics

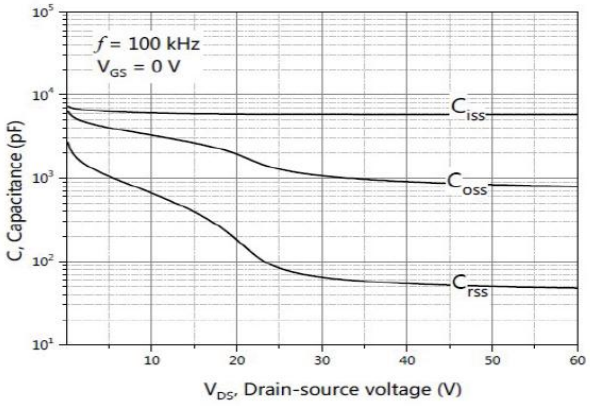


Figure3. Capacitance Characteristics

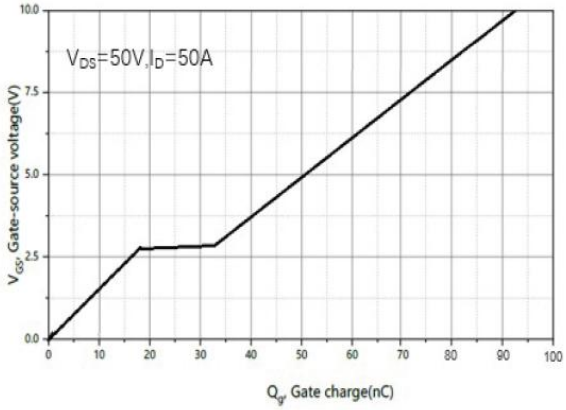


Figure4. Gate Charge

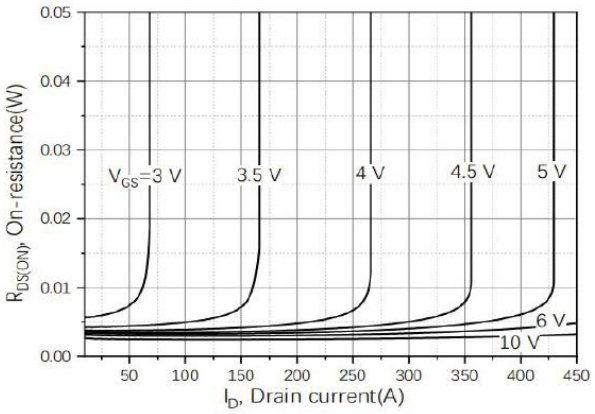


Figure5. Drain-Source on Resistance

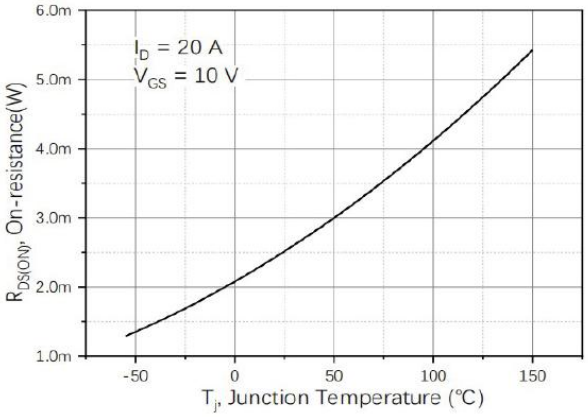


Figure6. Drain-Source on Resistance

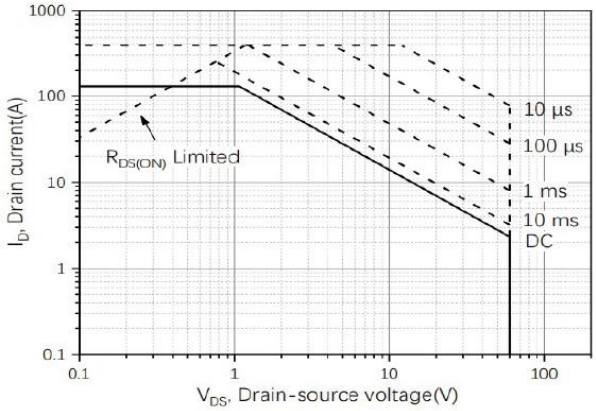


Figure7. Safe Operation Area

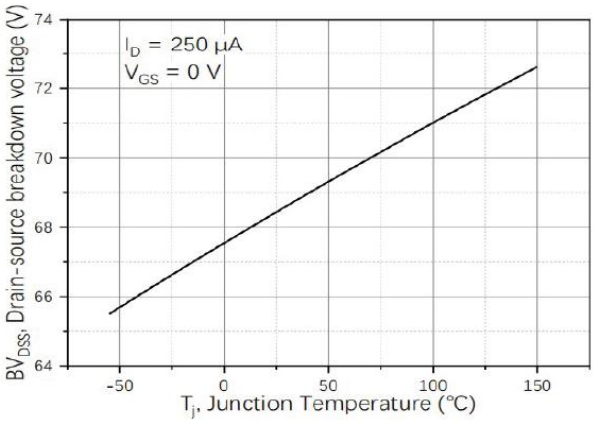


Figure8. Drain-source breakdown voltage

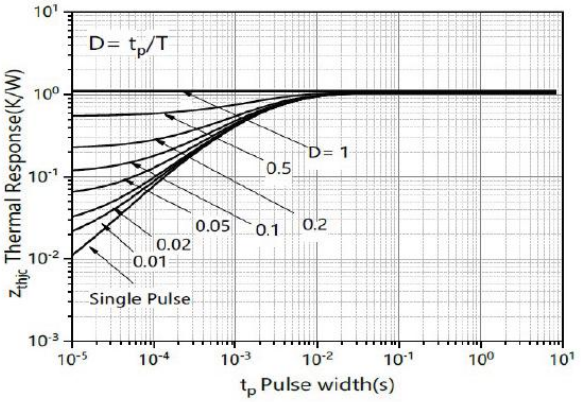


Figure 9.Transient thermal impedance

10. Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit & Waveforms

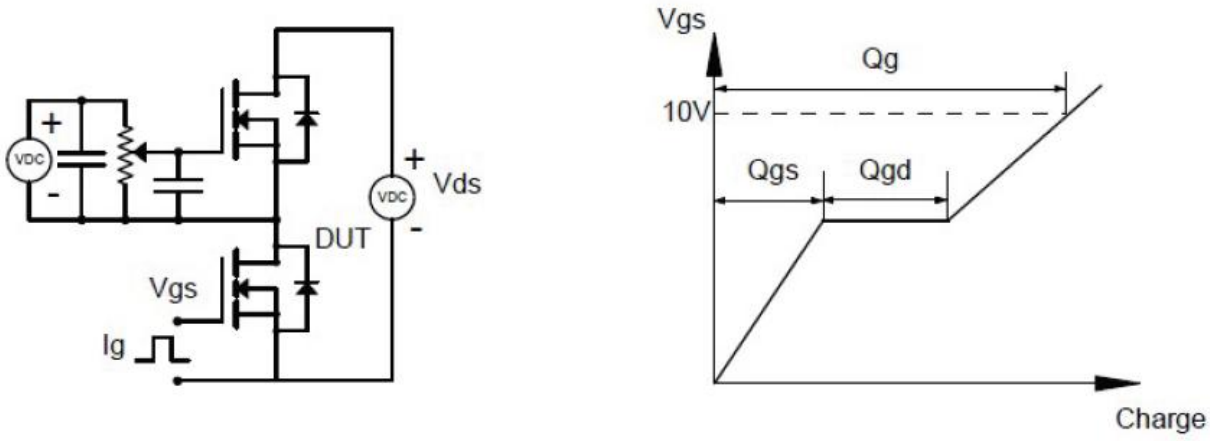


Figure B: Resistive Switching Test Circuit & Waveforms

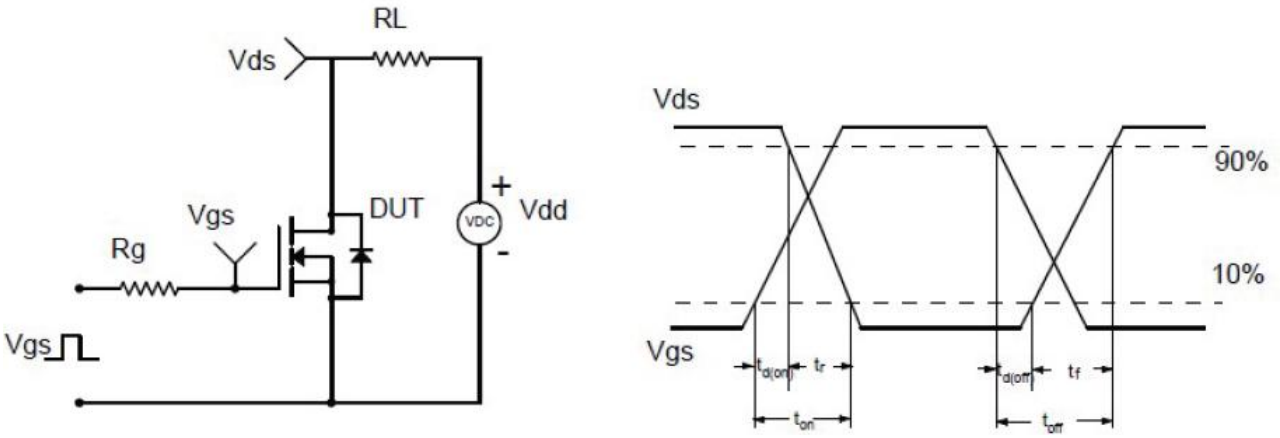


Figure C: Unclamped Inductive Switching (UIS) Test

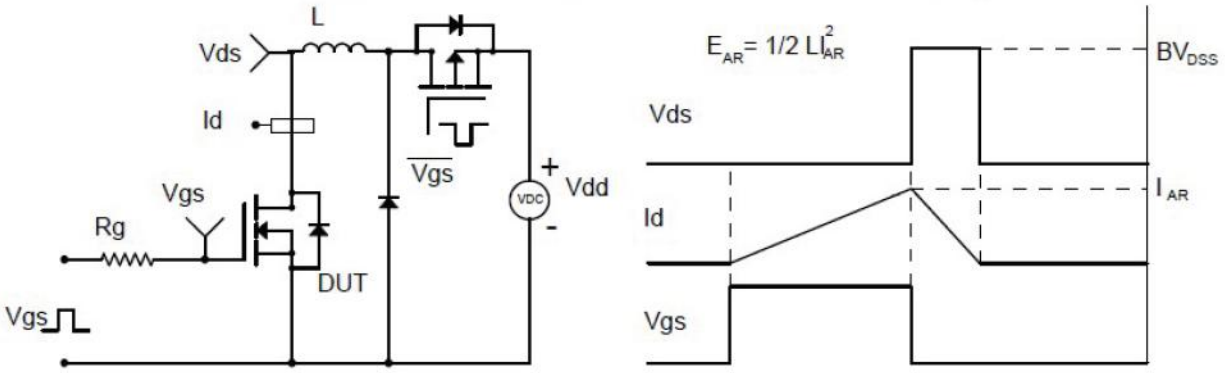


Figure D: Diode Recovery Test Circuit & Waveforms